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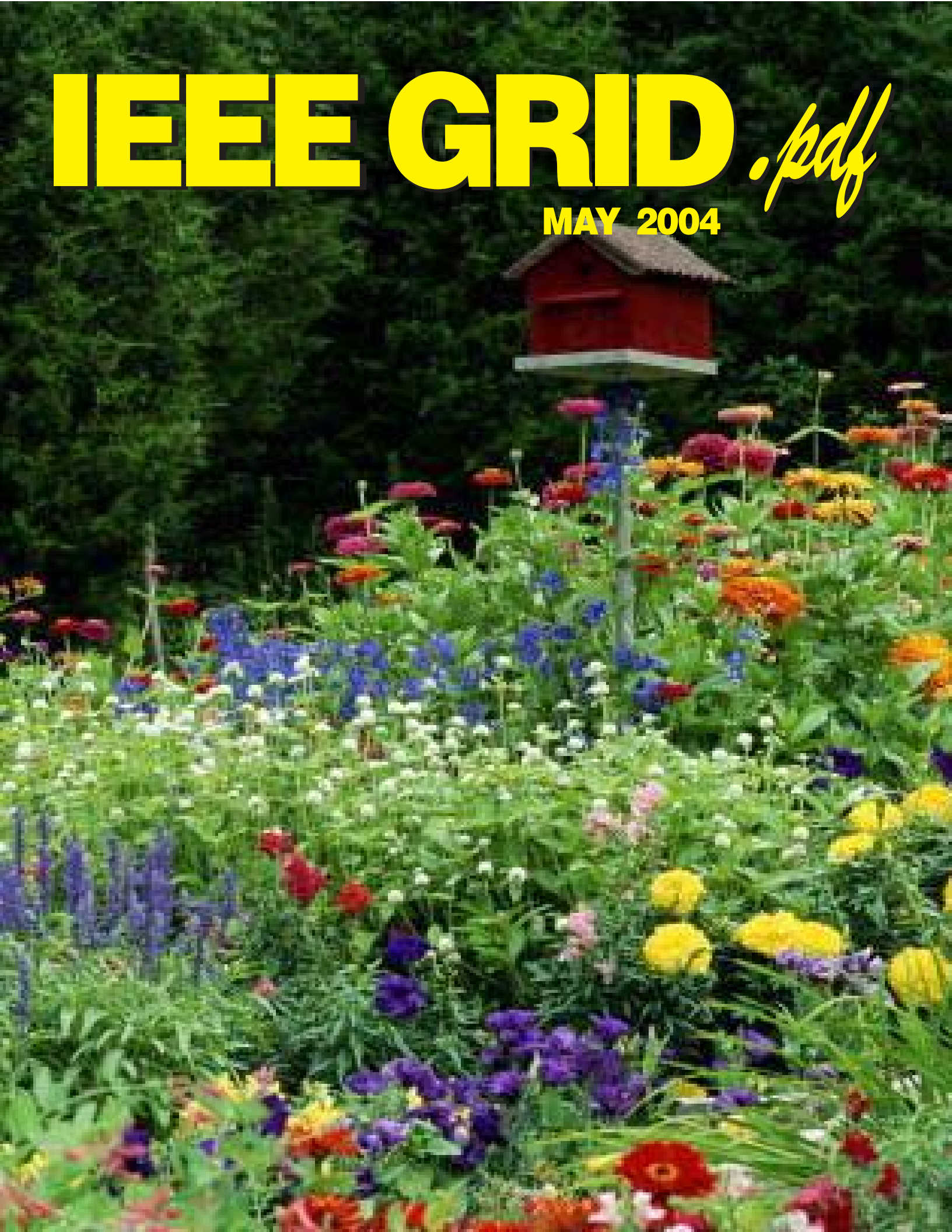

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IEEE Grid is the monthly newsmagazine of the San Francisco Bay Area Council of the Institute of Electrical and Electronics Engineers, Inc. As a medium for both news and opinion, the editorial objectives of IEEE Grid are to inform readers in a timely and objective manner of newsworthy IEEE activities taking place in and around the Bay Area; to publish the official calendar of events; to report on IEEE activities on a national and international scope; and to serve as a forum for comment on areas of concern to the engineering community by publishing contributed articles, invited editorials and letters to the editor.

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From the editor . . .

This is my farewell message. It isn't one I've wanted to write but like so many of you who have been laid off, downsized, or just plain let go due to the economy, I have been told that the cost-cutting this time around includes me.

This is my last issue of IEEE GRID and I'm dearly going to miss it. After almost 24 years of imposing and breaking deadlines, writing and editing thousands of paragraphs, working with countless society correspondents and numerous suppliers – typesetters, paste-up artists, printers, binderies, and the postal department. And then electronic distribution happened and now we have the Internet.

Finally, I suppose, that's all you need –the Internet. Not much call for an editor anymore.

Paul Wesling takes over this month as Webmaster for the Bay Area Council. All of you who have meeting notices to post, you'll now send them to Paul at p.wesling@ ieee.org.

That's a wrap for me. To all my IEEE friends, I say thank you for twenty-four unforgettable years.
Doug

NOTE: IEEE GRID.pdf is a monthly publication and is issued a few days before the first of the month. It is not updated after that. Please refer to the Online edition and interactive calendar for the latest information.

Electron Devices

FRIDAY MAY 7

FRIDAY MAY 7
SCV Electron Devices Society
Subject: **Half-day Symposium on Compact Modeling**
Speakers: Prof. R. Dutton, Prof. C. Yang, Prof. M. Miura-Mattausch, Dr. J. Xi, Dr. P. Bendix, Dr. N. Arora and Dr. P. Jansen
Time: Doors open at 1:00 p.m., presentations start at 1:30
Place: National Semiconductor, Building 31 Large Auditorium, 955 Kifer Road, Sunnyvale
RSVP: Info: ssaha@sst.com

Half-day Symposium on Compact Modeling

The Santa Clara Valley Chapter of the IEEE Electron Device Society, in collaboration with IEEE Compact Modeling Committee has organized a half-a-day symposium on Compact Modeling. The main focus area of the symposium is to learn from the invited distinguished speakers on the recent development in transistor level IC device model as well as IC interconnect model.

Some of the topics of presentation are: interconnect modeling for frequency-dependent crosstalk noise analysis; recent development in BSIM MOSFET models; HiSIM MOSFET models; and compact modeling for ESD optimization.

The panel of distinguished speakers is comprised of: Prof. Robert. W. Dutton, Stanford University; Prof. Cary Yang, Santa Clara University; Prof. Mitiko Miura-Mattausch, Hiroshima University, Japan; Dr. Jane Xi, University of California, Berkeley; Dr. Peter Bendix, LSI Logic Corp.; Dr. Narayan Arora, Cadence Design Systems; and Dr. Philippe Jansen, IMEC, Belgium.

SCV CPMT

WEDNESDAY MAY 12

WEDNESDAY MAY 12
SCV Components, Packaging & Manufacturing Technology
Subject: **Ultra-Small Miniaturization Technology**
Speaker: Bel Haba (Tessera)
Time: Seated dinner (vegetarian availalbe) served at 6:30 p.m., presentation at 7:30
Cost: $25 if reserved before May 8, $30 after and at the door — Prepay for dinner ($25) in one step from your PayPal account or Credit Card!
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expressway and Great America Parkway), Sunnyvale, (800) 888-3899
RSVP: allen.m.earman@intel.com - please reserve for "presentation-only" if not attending the dinner
Web: www.cpmt.org/scv

Ultra-small Miniaturization Technology

In recent years silicon technology has outpaced the packaging and testing technologies, leading to a serious speed bottleneck. Miniaturization (such as CSP technology) has led the way in the packaging field in helping the electrical and mechanical properties as well as improving the reliability. But further work is needed if we desire additional improvement in packaging technology. In his May 12 talk, Bel Haba will focus on the importance of miniaturization, whether it is stacking or system-in-a-package, and the importance of these various options will be highlighted. The electrical, thermal, and mechanical properties of such solutions will be discussed and illustrations of some applications will be discussed.

Dr. Belgacem (Bel) Haba is a Tessera Fellow working on developing new packaging technologies. He joined Tessera from SiliconPipe Inc., a high speed interconnect company where he was co-founder and vice president of engineering. Prior to that, Dr. Haba was manager of the packaging research and development division at Rambus. From 1991 to 1996, he had managed advanced research and development projects at the NEC Central Research Laboratories in Japan and earlier had worked for IBM at its T.J. Watson Research Center.

Dr. Haba got his bachelor's degree from the technical University of Algiers, Algeria in 1980. He holds two master's degrees — in applied physics and in materials science and engineering from Stanford University. He also earned a PhD in materials science and engineering from Stanford University in 1988. Dr. Haba holds 49 United States patents and over 80 worldwide patents and has authored more than 30 technical publications.

SCV Communications

WEDNESDAY MAY 12

WEDNESDAY MAY 12
SCV Communications Society
Subject: **VoIP Over the Internet: Is Toll Quality Achievable?**
Speaker: Dr. Mansour Karam (RouteScience Technologies, Inc.)
Time: Pizza and sodas at 6:00 p.m., presentation at 6:30
Fee: $1 donation to partially cover food cost
Place: National Semiconductor Credit Union, Bldg. 31, 955 Kifer Rd., Sunnyvale
RSVP: (required) rsvp@comsocscv.org
Web: http://www.comsocscv.org

VoIP Over the Internet: Is Toll Quality Achievable?

A main obstacle to the migration of voice communications from the public switched telephone network (PSTN) to voice-over-IP technology on the Internet has been a well-founded concern about the resulting degradation in call quality and reliability. VoIP has been demonstrated to work effectively on private IP networks where link quality is consistently high and where other IP traffic is tightly regulated.

The public Internet, however, was originally architected for "best effort" data communications, and is comprised of many different regional networks with varying link quality and completely unpredictable traffic flow. With the current move toward data/voice convergence, the expectations for IP infrastructure in terms of network reliability, as well as application quality and availability, have increased drastically.

Despite constant progress in these areas, the observed overall availability of typical Internet infrastructure rarely exceeds 99.9 percent, or "three nines". This is significantly short of the 99.999 percent "five nines" expectation that is customary in traditional circuit switched voice communications.

Recent technological advances can close this availability gap through an intelligent use of infrastructure monitoring, real-time call quality assessment and adaptive control that leverages the inherent redundancy in most networks.

This May 12 presentation will first present an overview of these technological advances, and will then go over case studies which demonstrate that toll quality voice communications is possible over the Internet, given the appropriate amount of network redundancy and adaptive control technology that is capable of taking advantage of this redundancy.

The speaker, Mansour Karam (M '98) received the B. Engineering degree in computer and communications engineering from the American University of Beirut, Beirut, Lebanon, in 1995 and the MS and PhD degrees in electrical engineering from Stanford University in 1997 and 2001, respectively. He is currently a technical lead at RouteScience Technologies. His research interests include the support of multimedia applications in wired and wireless networks and routing control over the Internet.

Mansour Karam is a member of the IEEE, and has co-authored the paper "Assessment of Voice over IP in Internet backbones," which was selected among the best 10 papers of Infocom 2002.

THURSDAY MAY 13

THURSDAY MAY 13
SCV-Microwave Theory & Techniques
Subject: **Calculating Image and LO Noise, and Spurious Levels in Frequency Converters**
Speaker: Bert Henderson (M/A-COM)
Time: Refreshments and social hour at 6:00 p.m., presentation at 7:00
Place: Agilent Technologies, Santa Cruz Conference Room, Building 50, 5301 Stevens Creek Blvd., Santa Clara
RSVP: Not required
Web: http://www.mtt-scv.org/mar_mtg.html

Calculating Image and LO Noise, and Spurious Levels in Frequency Converters

It is well known that placing broadband gain ahead of a mixer, where the amplifier has gain at both the desired and image input frequencies, will increase noise figure. This is due to the IF noise from the image adding with the IF noise from the desired input.

What is not as well known is how to correctly calculate the increase in noise figure as a function of the gain and noise figure of the amplifier and mixer. Similarly, AM noise on the LO input to the mixer can increase noise figure by also appearing at the IF output, and can produce unexpectedly high noise figure.

In addition, single- and two-tone spurious products can also degrade system performance. Accurate calculation of their levels requires advanced software; however, useful results can still be obtained from an older analytical approach that will be summarized. A representative system analysis using software developed by the presenter will be given to demonstrate the above analyses, and a free fully functional demonstration version of the software will be made available to attendees.

Bert Henderson has twenty-five years experience in microwave components and system design. Currently, he is a senior principal engineer with M/A-COM in San Jose, working on microwave and millimeter wave multifunction subassemblies. Prior to this he was with Bridgewave Communications and Endgate Corporation, both commercial communications start-ups, where he was responsible for the design of various millimeter wave front end systems. Prior to this he was with Watkins-Johnson Co. for fifteen years where he held various technical and leadership positions in RF and microwave design. He has a BSEE from University of California Davis, and MSEE from University of California at Berkeley. He has authored a number of technical papers, and has six patents.

SCV Solid State Circuits

THURSDAY MAY 13

TURSDAY MAY 13
SCV Solid State Circuits Society
Subject: **The Practice of Analog IC Design**
Speaker: Phillip E. Allen (Georgia Institute of Technology)
Time: Refreshments at 6:30 p.m., presentation at 7:00
Place: Cadence Design Systems, Bldg. 5, 2655 Seely, Ave., San Jose
RSVP: ssc_scv_rsvp@yahoogroups.com - for email reminder, send email to listserv@listserv.ieee.org
Web: http://www.ewh.ieee.org/r6/scv/ssc/

The Practice of Analog IC Design

In today's computer-driven, abstract level of circuit design, it becomes vitally important for the analog circuit designer to maintain a balanced viewpoint between the tools and concepts to be successful. This presentation focuses on the process of analog circuit design, particularly the design of analog integrated circuits. A historical perspective of the field of analog design will help understand the principles, concepts and techniques that have become masked in today's sophisticated computer-driven environment. The objective of this presentation will be to help understand what is analog IC design and how to accomplish successful and productive analog IC design.

The presentation will address the following questions: What is analog circuit design? What is the analog integrated circuit design process? What are the key principles, concepts and techniques for analog IC design? How can the analog IC designer enhance creativity and solve new problems in today's industrial environment?

Phillip E. Allen received the PhD in electrical engineering from the University of Kansas in 1970. He has worked with a number of companies including Lawrence Livermore Laboratory, Delco, Pacific Missile Range, Texas Instruments, Lockheed, and Schlumberger Well Services. Dr. Allen has taught at the University of Nevada, Reno, the University of Kansas, the University of California at Santa Barbara, and Texas A&M University. He has held the position of Schlumberger Chair Professor at Georgia Institute of Technology since 1984.

Continued next page

THURSDAY MAY 13

He has over 70 refereed publications in the area of analog circuits and integrated circuit design. He is the coauthor of Introduction to the Theory and Design of Active Filters (1980), Switched Capacitor Circuits (1984), CMOS Analog Circuit Design (1987, 2002), and VLSI-Design Techniques for Analog and Digital Circuits (1990) and is on the editorial boards of Integration-The VLSI Journal and Analog Integrated Circuits and Signal Processing. Dr. Allen was named a Fellow of the IEEE in 1992 "for contributions to electrical engineering education and microelectronics textbooks" and is a co-founder of the Georgia Tech Analog Consortium, which was established in 1990. Dr. Allen is a registered professional EE in the state of California.

His current research interests are the design of high performance analog circuits using submicron CMOS technology. Present research projects include frequency synthesizers, low-noise LC oscillators, filters including both discrete and continuous with high dynamic range, very high frequency bandpass filters at 1-5 GHz, analog-digital converters in the 8-10 bit, 100-1000 Msps range, and efficient power amplifiers using both CMOS and BiCMOS technology. Dr. Allen is also active in teaching short courses focused on analog design techniques for CMOS technology to professionals worldwide.

TUESDAY MAY 18

TUESDAY MAY 18
IEEE Consultants Network of Silicon Valley
Subject: **Networking, Networking, Networking: the IEEE CNSV's Way**
Speaker: Panel of Consultants Network Members
Time: Networking at 7:00 p.m., presentation at 7:30
Place: Sheraton Hotel, 1100 North Matilda Avenue, Sunnyvale – 408 745-6000
RSVP: Not required – Seating is limited, so arrive early

Networking, Networking, Networking: The IEEE CNSV's Way

Join us for this exciting meeting where some of our members will present and share what we can do to be successful in this new world in which consultants are living. There will be a panel of four seasoned professionals members of the Network: Art Rahman, Michael Collins, Gordon Force and Carl Angotti. This panel will discuss the current consulting environment present in 2004. They will focus on what marketing strategies have worked for panel members, and what has not worked, both last year and this year, then focus on the ever-changing business climate for engineering professionals. This will be a highly interactive meeting..

The slow recovery of high-tech sector of the U.S. economy which began last year, and the global competition represented by outsourcing has made us ponder several questions: Where do we go from here? If a task can be made routine, then it is very likely that it is going offshore, if it hasn't already. What then is the prescription for making your business more secure? What are some strategies we can use to ride the wave of offshore competition? The panel will share their ideas regarding all these questions.

At the end of this meeting, Art Rahman and the panel will present the possibility of forming a Special Interest Group (SIG) to help all of us get more assignments and income. One area of particular interest is that of becoming more entrepreneurial. We want to see if there is enough interest in such a SIG.

SCV Magnetics

TUESDAY MAY 18

TUESDAY MAY 18
SCV Magnetics Society
Subject: **Dynamics, damping and defects in thin ferromagnetic films**
Speaker: Dr. Robert D. McMichael (National Institute of Standards and Technology) Distinguished IEEE Lecturer for 2004
Time: Coffee and conversation at 7:30 p.m., presentation at 8:00
Place: Komag, 1710 Automation Parkway, San Jose
RSVP: Not required

Dynamics, Damping, and Defects in Thin Ferromagnetic Films

Modern disk drives can read and write bits every two nanoseconds, a time scale that is very similar to the magnetic damping time of the ferromagnetic metals used in the heads. The damping characteristics are also important for thermally driven magnetic noise in sensors.

Further, it seems likely that damping will limit data rates in MRAM since the magnetization in a memory cell must be allowed to settle between switching events. For all of these applications, measurements of damping are important, and these measurements are most commonly made by ferromagnetic resonance line width. The two problems that complicate measurements of damping by ferromagnetic resonance are 1) that defects contribute to the line width so that the line width is the combined effect of defects and damping, and 2) that the form of the damping itself is under some debate.

In this May 18 lecture, Dr. Robert D. McMichael will primarily discuss the role of defects in magnetization dynamics with an emphasis on the competition between interactions, which promote the collective behavior typified by spinwaves, and inhomogeneity, which promotes local behavior. An understanding of these effects allows one to use line width data to characterize damping and inhomogeneity separately. He will show examples of line width data and modeling from nominally uniform films, exchange biased films, films with wavy substrates and films with nonuniform magnetization.

Patterning is perhaps the ultimate form of magnetic inhomogeneity in a thin film. Unlike the spin-wave normal modes of a continuous film,the normal modes of patterned elements are shape and size dependent. The dynamic properties can be addressed using available micromagnetic modeling software to obtain images of the normal mode precession patterns.

Robert D. McMichael received the BS degree in engineering-physics from Pacific Lutheran University in 1985, and the MS and PhD degrees in physics from Ohio State University in 1990. In 1990, he was awarded a National Research Council postdoctoral associateship at the National Institute of Standards and Technology, and he has continued on in the Magnetic Materials Group of the Materials Science and Engineering Laboratory of NIST. His research interests have touched on a diverse set of topics including nonlinear magnetization dynamics, ferromagnetic resonance, magnetic refrigeration, hysteresis modeling, giant magnetoresistance, exchange bias, computational micromagnetics and magnetization dynamics. He currently serves as leader of the Nanomagnetodyamics project in NIST's Metallurgy Division.

Bob serves on the editorial board of IEEE Transactions on Magnetics, and on the Advisory Committee for the MMM conference. He created the logos of several recent MMM conferences.

WEDNESDAY MAY 19

WEDNESDAY MAY 19
SCV Engineering in Medicine & Biology Society
Subject: **Optical Biopsy in Gastroenterology**
Speakers: Prof. Jacques Van Dam and Prof. George Springer (Stanford University)
Time: Dinner at 6:15 p.m., presentation at 7:30
Place: Dinner in the Stanford Hospital Cafeteria, presentation in Room M114 of the Stanford Medical School
RSVP: Not required
Web: http://ieee.org/scv/embs/

Optical Biopsy in Gastroenterology

Dr Van Dam will speak on the indications for small bowel imaging, the limitations of standard endoscopic and radiographic techniques, and then a brief overview of the GIVEN capsule technology and recent data on its clinical utility. (The GIVEN capsule is a swallowable, disposable camera system for endoscopic use.)

Dr Springer will discuss recent work on a maneuverable camera capsule.

Dr Van Dam is professor of medicine at Stanford University School of Medicine and Clinical Chief of the Division of Gastroenterology and Hepatology at Stanford University Medical Center. He received his M.D. and Ph.D. degrees from Georgetown University School of Medicine and completed his postgraduate medical training at Harvard Medical School, where he remained on the faculty for more than ten years. Dr Van Dam is an NIH-funded investigator and is the author of more than 300 scientific papers, reviews and abstracts.

OEB Communications Society

THURSDAY MAY 20

THURSDAY MAY 20
OEB Communications Society
Subject: **DSP for Packet Voice Telephony**
Speaker: Dr. Krishna Vemireddy (LSI Logic)
Time: Pizza at 6:30 p.m., presentation at 7:00
Place: Bishop Ranch 1, 6101 Bollinger Canyon Road, San Ramon (just off I-680)
RSVP: (by 5/19) oeb@comsoc.org
Web: http://www.comsoc.org/oeb/

DSP for Packet Voice Telephony

We are presently in the midst of an irreversible transition of the telephone network from a circuit-switched to a packet-switched framework. From its initial corporate moorings (where telephony is supported over internal networks), Voice over Internet Protocol (VoIP) use is now surging into the residential market place, as evidenced by recent worldwide announcements from major telephony service providers and cable multi-system operators.

In this May 20 talk Dr. Krishna Vemireddy considers the impact this evolution has in terms of digital signal processing (DSP) requirements at various points of the network. He will focus on the customer premises equipment (CPE), while making a brief reference to packet voice gateways. CPEs for packet voice telephony range from a simple single-line telephone to private branch exchanges (PBX) catering to hundreds of users.

While the choice of protocol (SIP, H.323, H.248) and its actual implementation is a crucial factor, this talk will be confined to how various elements of the DSP layer need to be configured to ensure quality and inter-operability in a cost-effective manner. This layer is the foundation over which higher layer protocols and quality-of-service mechanisms facilitate deployment of VoIP across different physical media (DSL / cable modems, Wi-Fi, etc.).

The talk will consider the following key voice processing aspects of the DSP layer: voice compression alternatives; requirements for line echo cancellation; support for various call progress and signaling tones; and packet loss concealment. Specifically, these functions will be presented in the context of end-user IP telephones as well as that of a multi-user IP-PBX. The associated processing requirements will also be considered. Finally, some trends for the future will be highlighted.

Continued next page

THURSDAY MAY 20

Krishna Vemireddy (V V K) is a DSP solutions architect at LSI Logic. He holds a PhD from the Indian Institute of Science (IISc) and has over 17 years of industrial R&D exposure. Prior to LSI Logic, he has worked in Bangalore, India at IISc, Bharat Electronics, Ncore Technology (now Encore Software), and Signion Systems. His primary interests include adaptive filters and their applications.

The chapter will continue its feature at the meeting of providing some networking time for those that want to stand and make a brief announcement. If you're looking for a new position, have a position to fill, want to let us know that your new start-up is ready for business, or have a similar announcement, bring your resumes, job descriptions or company brochures and be prepared to make a match. Please keep your statements brief, so we'll have time for everyone. There will be time before and after the formal meeting for one-on-one discussions.

WEDNESDAY MAY 26

WEDNESDAY MAY 26
SCV Engineering Management Society
Subject: **Resolving Conflict on Geographically Dispersed Teams**
Presenter: Jenny Brandemuehl
Subject: **Sustainable Systems for Off-the-Grid Communities**
Speaker: Danial Pitt (Santa Clara University)
Time: Forum at 6:00 p.m., dinner at 7:00, after dinner presentation at 7:45
Place: Wyndham Garden Hotel, 1300 Chesapeake Terrace, Sunnyvale - off Lawrence Expressway/Caribbean Drive at Hwy 237
RSVP: http://www.ieee-scv-ems.org
Cost: (with reservations by Friday May 21) $25 (IEEE member), $30 (non member), $5 surcharge thereafter. (Cash or check at the door). Student IEEE members - $5.
Info: Rich Hendrickson, 408 203-3462.

Continuing Series on Remote and Offshore Engineering Management

The Santa Clara Valley Engineering Management Society presents a before-dinner forum on challenges in diversity of virtual teams. Following networking and a sit-down dinner, the after-dinner topic will be on sustainable systems for off-the-grid communities.

Before-Dinner presentation -

Effective Virtual Meetings

When a team is diverse in work style and culture, the potential for conflict is high. Add virtual work to the mix and some unique team problems can develop. Jenny Brandemuehl will describe the common pitfalls that geographically dispersed teams experience when conflict arises by describing each stage of a conflict. She will also discuss how different conflict approaches manifest itself in virtual team behaviors and communication and offer tools and solutions for effectively resolving conflicts.

Jenny is co-founder of Virtual Connection, a company that provides tools, workshops and coaching to improve the performance of geographically dispersed teams. She has worked for 18 years in a variety of positions such as change management consulting, information technology and human resources management at Hewlett Packard, National Semiconductor, and SMC. Jenny led several global program teams at Hewlett Packard and is currently co-authoring an article on virtual team conflict.

After-Dinner presentation -

Sustainable Systems for Off-the-Grid Communities

Daniel Pitt will be presenting the vision for Santa Clara University for intelligent sustainable systems. A few examples of these systems will be presented for the residential and community levels applied to societies in the first and third worlds.

Continued next page

WEDNESDAY MAY 26

Daniel A. Pitt is dean of the School of Engineering at Santa Clara University, the Jesuit University of Silicon Valley. The School, founded in 1912, offers over 500 undergraduates an engineering education characterized by small classes, close faculty contact, innovative projects, interaction with Silicon Valley companies, and life-lasting perspectives from coursework in liberal arts, religion, and ethics. To its 800 graduate students, the school offers the opportunity to pursue M.S. and Ph.D. degrees while they hold down jobs by scheduling all classes outside the 9-5 workday.

Dr. Pitt became dean of the school in 2002 after a 23-year career in industry. From 1997 to 2002 Pitt served as vice president of Bay Networks and, following its acquisition, Nortel Networks, running the Bay Architecture Lab at Bay and the Technology Center at Nortel. His organization, spread over nine cities in five countries, developed new protocols, architectures, and product concepts for networking and telecommunications technologies.

Throughout his tenure at Bay and Nortel Pitt held responsibility for university partnerships as well. From 1992 to 1997 Dr. Pitt managed technology development for residential broadband services at Hewlett Packard Labs in Palo Alto, including the architecture for the company's video server, which led the market in the mid 1990s. From 1979 to 1992 he was with IBM, leading the architecture and worldwide standardization of local area networks, in particular the token ring LAN, source routing, and AAL type 2, in Research Triangle Park, North Carolina, and managing the development of the company's first ATM architectures and components, including the invention of ATM LAN emulation, at the research lab in Rueschlikon, Switzerland.

Dr. Pitt received a BS in mathematics (magna cum laude) from DukeUniversity and an MS and PhD in computer science from the University of Illinois. He taught as an adjunct professor of computer science and electrical engineering at Duke University and the University of NorthCarolina and has served as a member of the industrial advisory board of the department of electrical engineering and computer sciences at the University of California, Berkeley, as well as a member of the advisory board of the institute for computer communications and applications at the Swiss Federal Institute of Technology, Lausanne.

Professional Services Marketplace - d.davolt@ieee.org for information